Claims 12, 16, and 18 stand rejected under 35 U.S.C. 112, first paragraph. The Examiner asserts that the phrase "a low dielectric constant sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads . . . " is not supported in the specification. This phrase appears in Claim 16 and in a modified form in Claim 18. Applicant submits that this claim language is supported in the paragraph on page 10 of the instant specification at line 15 when read in conjunction with Figure 4a. That paragraph contains the following statement: "The coating, or sheath 45 which has been applied after the wire bonding process, extends onto both the chip surface and the portion of the lead where the wire is attached." Figure 4a also makes clear that the sheath 45 covers substantially only the wire and the portion of the lead where the wire is attached. The sheath therefore does not cover other portions of the chip and the conductive leads. Those things are covered by encapsulant 44 rather than by the sheath 45. The Examiner points out that in Figure 4a, the sheath 45 covers a portion of the chip. Applicant acknowledges that fact, but Claims 16 and 18 says "said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip." Therefore, the cited claim language is consistent with and is supported by the specification.

With regard to Claim 12, the Examiner objects to the "open cavity" referred to in that claim. Support for that portion of Claim 12 is found in the paragraph bridging pages 8 and 9 of the specification. On line 26 of page 8, the specification reads as follows: "[f]igure 2b is a model of a device having the same dimensions, but housed in the *cavity* of a shell 26 having a dielectric constant of 4.0. The cavity and space between wires is filled by air 25 having a dielectric constant of 1.0. This model is representative of a *cavity* package." Applicant submits that "open" is equivalent to "filled by air" in the above-quoted passage. Therefore, Applicant respectfully submits that the term "open cavity" is supported in the specification.

Claims 1, 12, 16, and 18 stand rejected under 35 U.S.C. 112, second paragraph. The Examiner asserts that the term "substantially" in claims 1, 12, 16 and 18 render the claims indefinite. Applicant disagrees. MPEP 2173.05(b) states that "[t]he fact that claim language, including terms of degree, may not be precise, does not automatically render the claim indefinite under **35 U.S.C. 112**, second paragraph. *Seattle Box Co., v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 221 USPQ 568 (Fed. Cir. 1984). Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification." The language "said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip" indicates that essentially only the wire and wire connections are covered with the sheath. Some of the material used to form the sheath may settle down to cover a portion of the chip around the pads as shown in Figure 4a, hence Applicant's use of the word "substantially" in indicating that only the wire and wire connections are covered. Applicant therefore respectfully submits that the claim language when read in conjunction with the specification and Figure 4a is clear and definite to one skilled in the art.

Claims 1, 3, 10, and 11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (U.S. Patent No. 6,013,109) in view of Casto (U.S. Patent No. 5,172,214). Claim 1 includes the feature of "a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads." Neither Choi nor Casto disclose or suggest such a feature. In citing Casto, the Examiner referred to col. 1, line 30 to col. 4, line 21 of Casto, which is essentially the entire text of the patent other than the claims. At col. 1, lines 39-46, and elsewhere, Casto is referring to densely-spaced *leads*, not wire bonds. Since the proposed combination of references fails to teach or suggest all of the claimed features, Applicant respectfully submits that Claim 1 is patentable over that combination. Claims 3, 10, and 11 depend from Claim 1 and are therefore patentable over the combined references for at least the reasons presented above.

Claims 2, 4-9, and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Casto and further in view of Eysermans (U.S. Patent No. 4,048,670). Claim 2 depends from Claim 1. As stated above, Claim 1 includes the feature of "a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads." Neither Choi nor Casto nor Eysermans teach or suggest such a feature. Therefore, Applicant submits that Claim 1, and Claims 2, 4-9 and 13, which depend therefrom, are patentable over the combined references.

Claims 14-15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Casto and further in view of Featherby, et al. (U.S. Patent No. 6,368,899). Claim 1 is distinguishable from Choi in view of Casto for the reasons presented above. Featherby does not cure the deficiencies of Choi and Casto. In Featherby's Figure 12, note that bond wires 18 are not substantially parallel or closely-spaced to the extend that mutual capacitance would be significant. Claims 14 and 15 depend from Claim 1 and are therefore patentable over Choi in view of Featherby for the reasons presented above. In addition, Claim 14 includes the feature wherein "said cavity package shell comprises ceramic." The Examiner refers to Featherby's Figure 8 as including a cavity package shell. However, at col. 12, lines 10-15, Featherby refers to element 12 as a plastic package. It is therefore clear that the package of Figure 8 is simply a plastic package with a duplex coating, and is not a cavity package. The same reasoning applies to the rejection of Claim 15. Featherby does not disclose or suggest a cavity package.

Claim 12 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Kim, et al. (U.S. Patent No. 5,801,074). Applicant respectfully submits that there is no motivation in the references for the proposed combination. Choi's polyimide type coating material that covers the chip, lead frame paddle, bond wires and bond paste servers as a buffering member

between those components and the molding resin 29. A cavity package lacks the complete covering of mold resin described in Choi. Therefore, one skilled in the art would receive no motivation to apply the coating method of Choi to the cavity package taught by Kim. Accordingly, Applicant respectfully submits that Claim 12 is patentable over Choi in view of Kim.

Claim 16 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Kim and further in view of Kobayashi (U.S. Patent No. 4,821,148). Claim 16, as amended, includes the feature of "a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads." As indicated above with respect to Claim 1, Choi does not teach or suggest such a feature. Neither Kim nor Kobayashi teach or suggest such a feature. The proposed combination being deficient in teaching or suggesting all of the claimed features, Applicant respectfully submits that Claim 16 is patentable over that combination.

Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Eysermans, Kim, and Kobayashi. Applicant respectfully submits that one skilled in the art would receive no motivation from these references for the proposed combination. Eysermans's foamed polyurethane is used as a cushioning material at the bottom of a cup in which a semiconductor chip is placed. Eysermans does not teach or suggest coating bond wires with such a material, and in his Figures 4, 6, 7, and 8, his bond wires are not coated. There would be no motivation for the skilled artisan to combine Eysermans's teaching of a foamed cushioning material with the teachings of Choi, Kim, and Kobayashi. Therefore, Applicant respectfully submits that Claim 18 is patentable over the proposed combination.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-16 and 18. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

16. (amended) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including;

a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads,

a low dielectric constant sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads, and

a mold compound encasing the chip, sheathed wires, and leads.

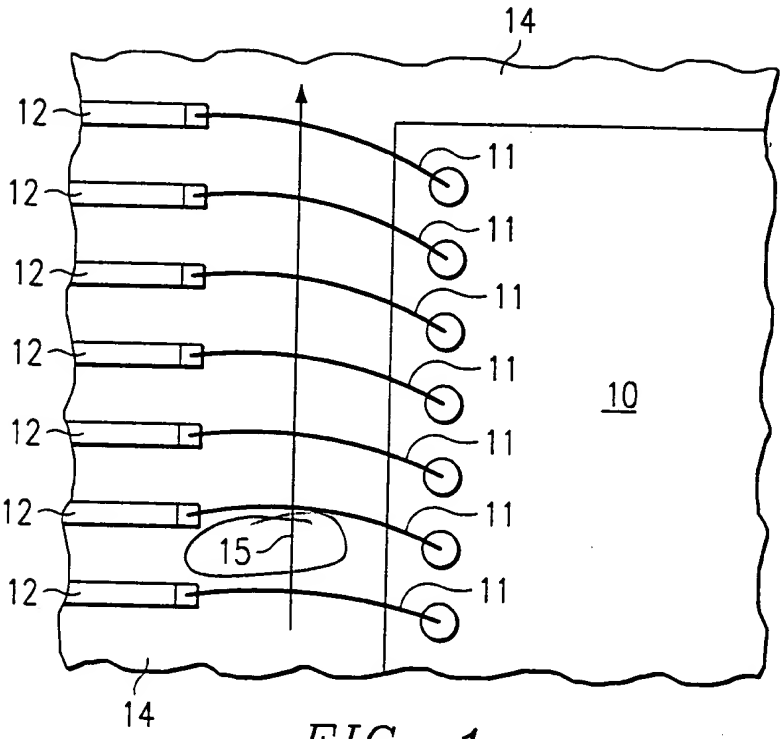

FIG. 1a
(PRIOR ART)

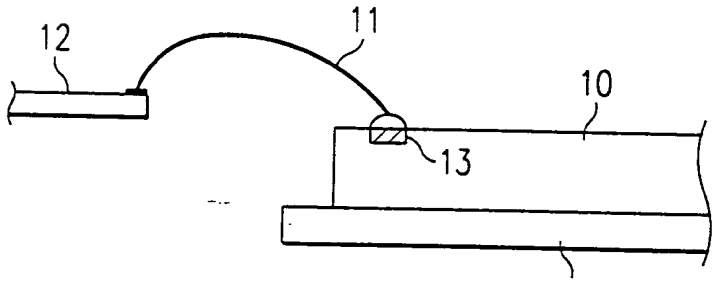

FIG. 1b
(PRIOR ART)

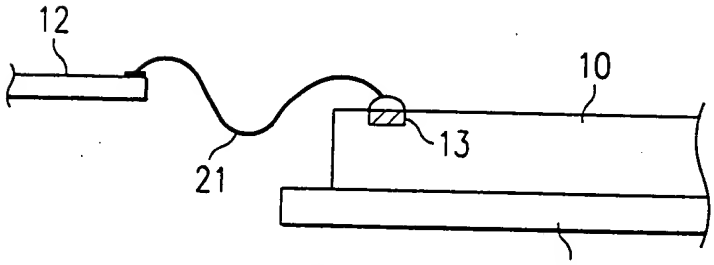

FIG. 1c
(PRIOR ART)